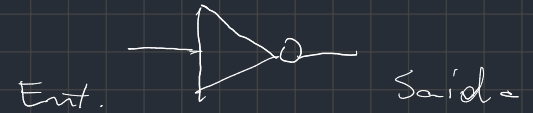
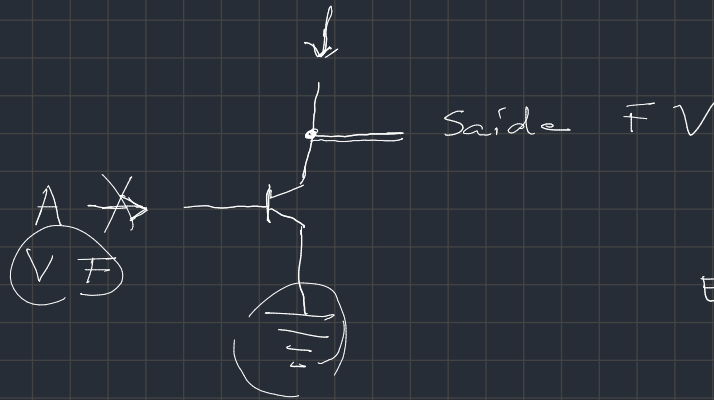


┌ Verdadeira (V)
 0 1
 └ Falso (F)

Portas lógicas

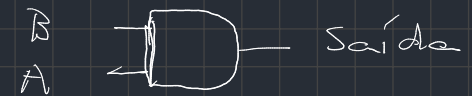
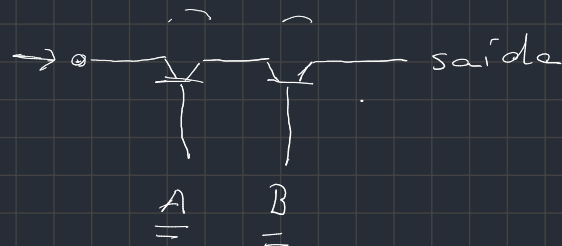
Não (Not)

| Entrada | Saída |
|---------|-------|
| V | F |
| F | V |

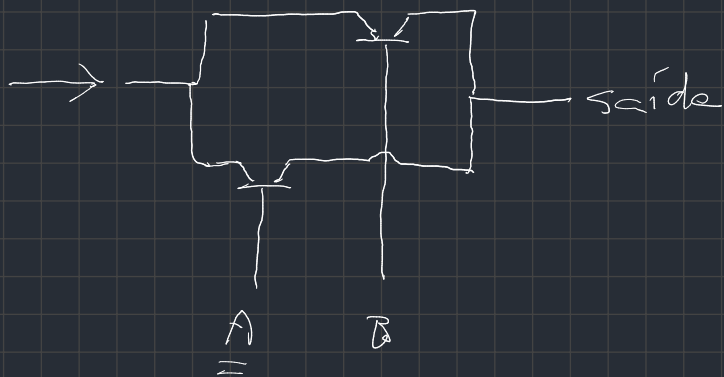


E And

| Entradas | | Saída |
|----------|---|-------|
| A | B | |
| V | V | V |
| V | F | F |
| F | V | F |
| F | F | F |



OU (OR)

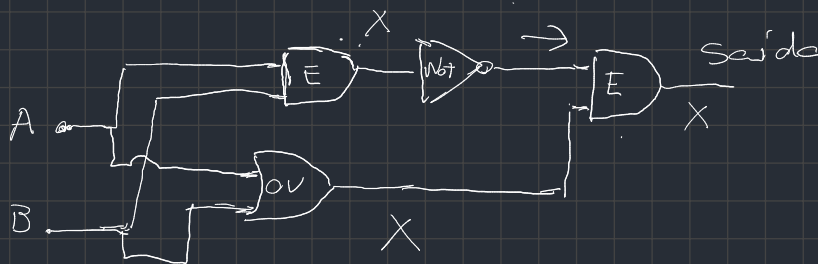


| Entradas | | Saída |
|----------|---|-------|
| A | B | |
| ✓ | ✓ | ✓ |
| ✓ | F | ✓ |
| F | ✓ | ✓ |
| F | F | F |



OU exclusivo XOR

| Entradas | | Saída | |
|----------|---|-------|---|
| A | B | | |
| ✓ | ✓ | F | ✓ |
| ✓ | F | ✓ | ✓ |
| F | ✓ | ✓ | ✓ |
| F | F | F | ✓ |



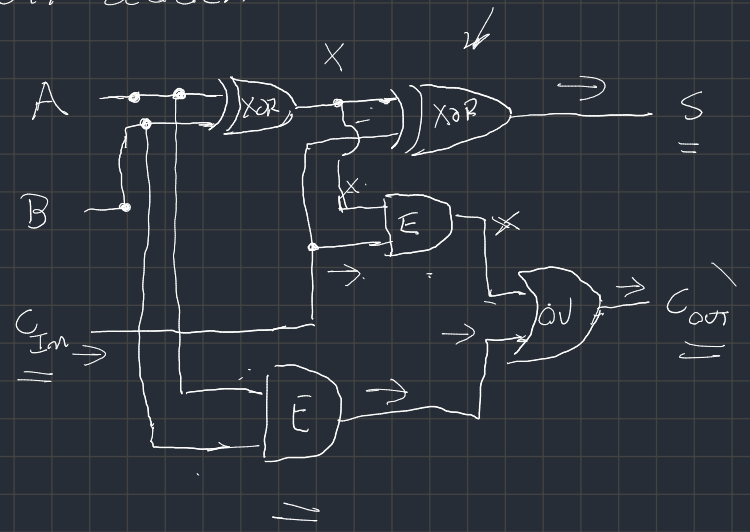
$$\begin{array}{r} 1\ 1 \\ 1\ 9\ 7 \\ \hline 0\ 4\ 5 \\ 2\ 4\ 2 \end{array}$$

$$\begin{array}{r} 0\ 1 \\ \hline 0\ 1\ 0 \\ \downarrow \\ 1\ 1\ 1\ 0 \end{array}$$

$$\begin{array}{r} C_{out} \\ \downarrow \\ 1\ 1\ 1 \\ \hline 1\ 0\ 1 \\ 0 \end{array}$$

$$\begin{array}{l} 10_b \\ = \\ 11_b = 3_d \\ = \end{array}$$

Full adder



| A | B | C _{in} | S | C _{out} |
|---|---|-----------------|---|------------------|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 |

111011

$$\begin{array}{r} 1 \\ 1 \\ 1 \\ \hline 0 \end{array}$$

